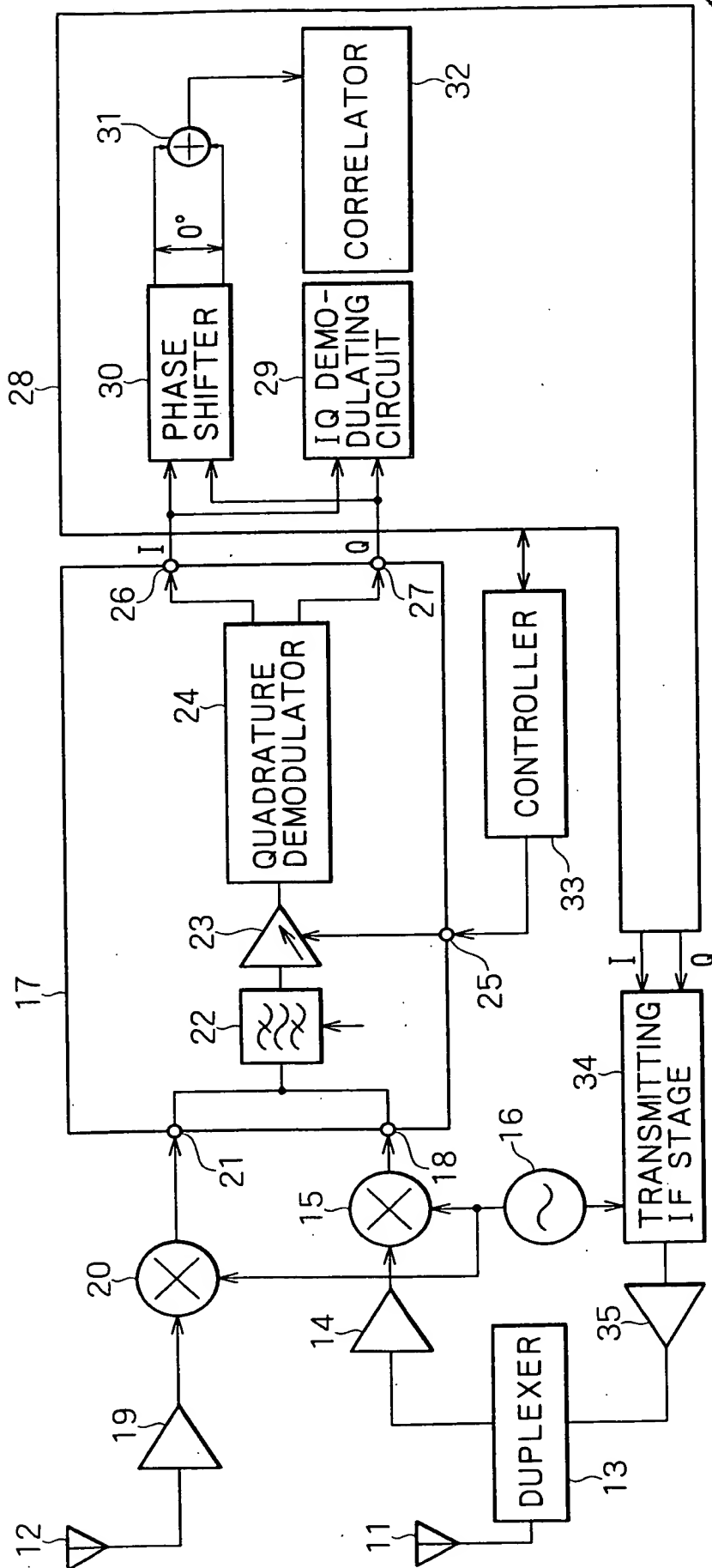


FIG. 1



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FIG. 2

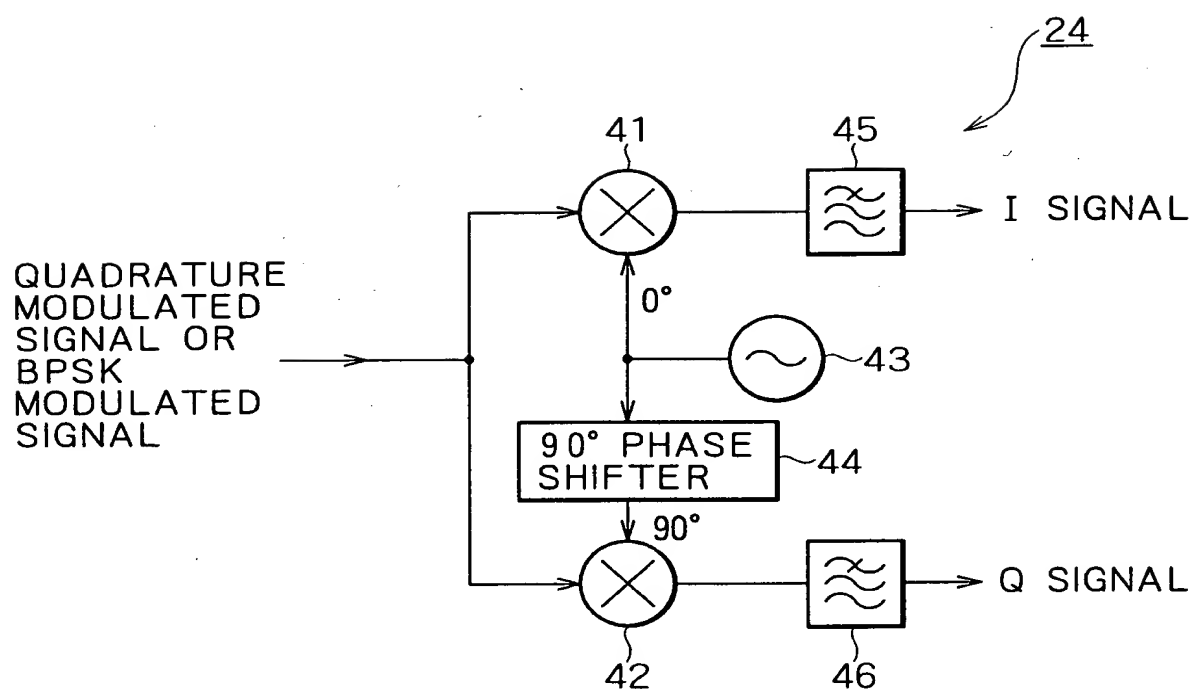




FIG. 3

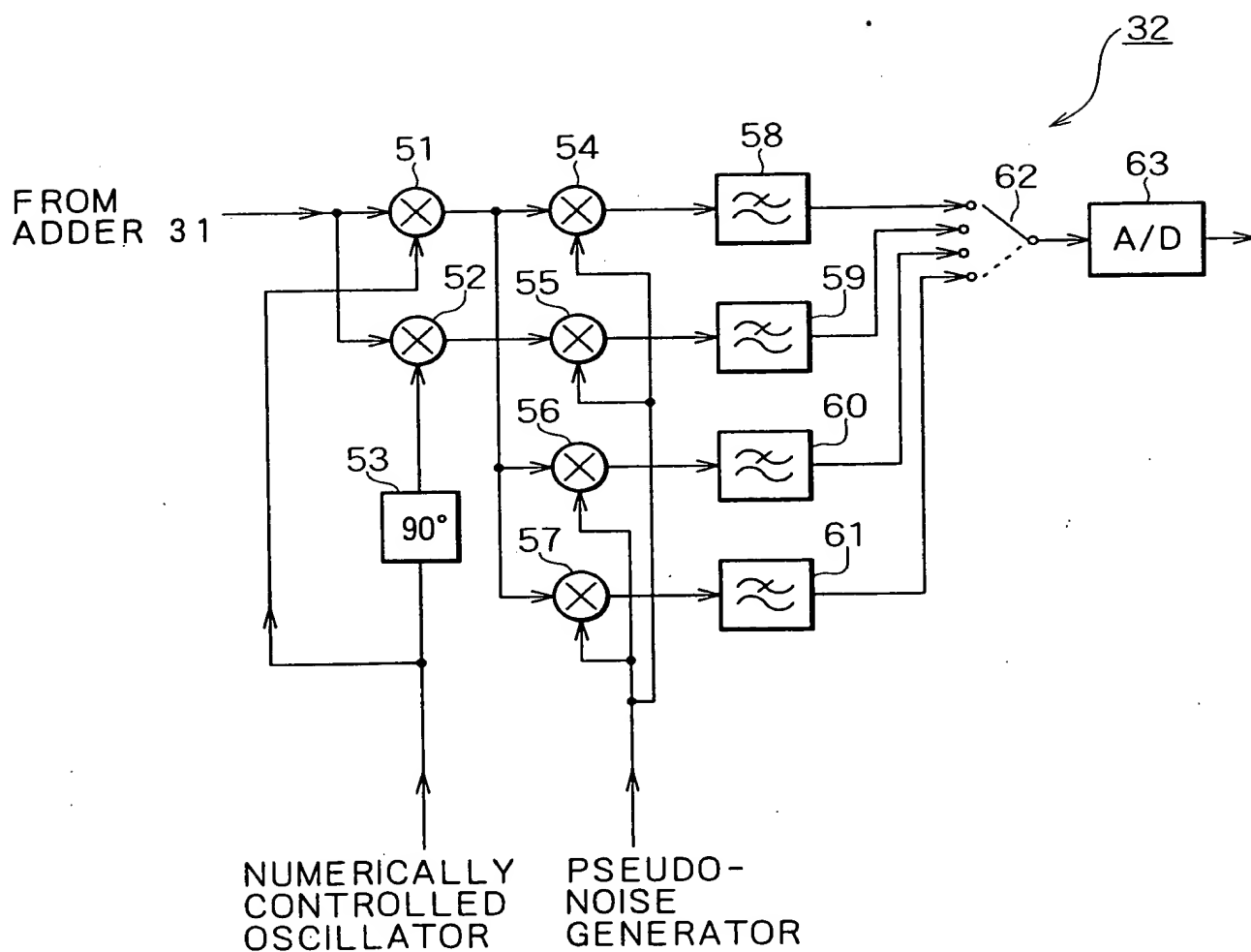


FIG. 1 is a block diagram of a GPS receiver system. The system includes an antenna (10) connected to a low noise amplifier (12). The output of the amplifier is filtered by a bandpass filter (14) and then amplified by a variable gain amplifier (16). The output of the variable gain amplifier is split into two paths. One path goes through a 0-degree phase shifter (18) and a mixer (20) to produce the I channel signal. The other path goes through a 90-degree phase shifter (22) and a mixer (24) to produce the Q channel signal. Both I and Q signals are then fed into a correlator (32) and an IQ demodulating circuit (29). The correlator output is connected to a processor (34). The processor is also connected to a GPS data source (36) and a display (38). The display shows the signal strength and the position of the receiver.

FIG. 5

